



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/622,372	01/12/2001	Tomoki Sekiguchi	ASA-904	3506
24956	7590	07/22/2004	EXAMINER	
MATTINGLY, STANGER & MALUR, P.C. 1800 DIAGONAL ROAD SUITE 370 ALEXANDRIA, VA 22314			MASKULINSKI, MICHAEL C	
		ART UNIT	PAPER NUMBER	
		2113	12	
DATE MAILED: 07/22/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 09/622,372	Applicant(s) SEKIGUCHI ET AL.
Examiner Michael C Maskulinski	Art Unit 2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

1)  Responsive to communication(s) filed on 10 May 2004.  
2a)  This action is FINAL.                  2b)  This action is non-final.  
3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## **Disposition of Claims**

4)  Claim(s) 1-15 is/are pending in the application.  
    4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5)  Claim(s) \_\_\_\_\_ is/are allowed.

6)  Claim(s) 1,4,6,9,12 and 13 is/are rejected.

7)  Claim(s) 2,3,5,7,8,10,11,14 and 15 is/are objected to.

8)  Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## **Application Papers**

9)  The specification is objected to by the Examiner.

10)  The drawing(s) filed on \_\_\_\_\_ is/are: a)  accepted or b)  objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)  The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a)  All b)  Some \* c)  None of:  
1.  Certified copies of the priority documents have been received.  
2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)  Notice of References Cited (PTO-892)  
2)  Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3)  Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 5.  
  
4)  Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_ .  
5)  Notice of Informal Patent Application (PTO-152)  
6)  Other: \_\_\_\_ .

**Final Office Action**

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 4, 6, 9, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goodrum et al., U.S. Patent 6,032,271, and further in view of Armstrong et al., U.S. Patent 6,182,248 B1.

Referring to claims 1, 6, and 12:

In column 86, lines 56-64, Goodrum et al. disclose that the bus watcher (manager) can detect for a hang condition on the secondary PCI bus. However, Goodrum et al. don't explicitly disclose generating an I/O bus signal, which makes the I/O bus fail. In column 2, lines 3-22, Armstrong et al. disclose a fault- injecting tool for injecting a fault on a bus. It would have been obvious to one of ordinary skill at the time of the invention to include the fault-injecting tool of Armstrong et al. into the system of Goodrum et al. A person of ordinary skill in the art would have been motivated to make the modification because *once an error is successfully injected, the operation of fault isolation and recovery facilities for the bus being tested may be observed to ascertain whether they are properly functioning* (see Armstrong et al.: column 2, lines 22-25).

Further, in column 86, lines 56-64, Goodrum et al. disclose that if a hang condition is detected, the bus watcher sets a bus hang pending bit, which causes the

SIO (I/O bus manager) to power down the slots on the secondary PCI bus and a non-maskable interrupt (NMI) to be transmitted to the CPU (transmitting an I/O bus signal from said manager to an I/O bus manager in said computer at a predetermined point of time to inform said I/O bus manager of occurrence of an I/O bus fault to thereby make said I/O bus manager initialize said I/O bus). The CPU responds to the NMI by invoking an NMI routine to isolate the slot(s) causing the hang condition. Once identified, the defective slot(s) are disabled or powered off (and then informing a CPU in said computer of said I/O bus fault as an interruption to be processed by an OS operated by said CPU).

Referring to claims 4 and 9, in column 87, lines 57-64, Goodrum et al. disclose that the NMI handler calls a BIOS isolation handler for isolating the defective slot or slots. Otherwise, other NMI procedures are called (wherein said OS carries out fault processing in response to said interrupt).

3. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goodrum et al., U.S. Patent 6,032,271, and further in view of Pitroda et al., U.S. Patent 4,149,038.

Referring to claim 12:

In column 86, lines 56-64, Goodrum et al. disclose that the bus watcher (manager) can detect for a hang condition on the secondary PCI bus. However, Goodrum et al. don't explicitly disclose generating an I/O bus signal, which makes the I/O bus fail. In column 2, lines 64-68 continued in column 3, lines 1-2, Pitroda et al. disclose a fault- injecting tool for injecting a fault on a bus. It would have been obvious

to one of ordinary skill at the time of the invention to include the fault-injecting tool of Pitroda et al. into the system of Goodrum et al. A person of ordinary skill in the art would have been motivated to make the modification because the operation of fault isolation and recovery facilities for the bus being tested may be observed to ascertain whether they are properly functioning (see Pitroda et al.: column 9, lines 10-38).

Further, in column 86, lines 56-64, Goodrum et al. disclose that if a hang condition is detected, the bus watcher sets a bus hang pending bit, which causes the SIO (I/O bus manager) to power down the slots on the secondary PCI bus and a non-maskable interrupt (NMI) to be transmitted to the CPU (transmitting an I/O bus signal from said manager to an I/O bus manager in said computer at a predetermined point of time to inform said I/O bus manager of occurrence of an I/O bus fault to thereby make said I/O bus manager initialize said I/O bus). The CPU responds to the NMI by invoking an NMI routine to isolate the slot(s) causing the hang condition. Once identified, the defective slot(s) are disabled or powered off (and then informing a CPU in said computer of said I/O bus fault as an interruption to be processed by an OS operated by said CPU).

Referring to claim 13, in column 6, lines 28-44, Pitroda et al. disclose that a remote terminal interface allows the control complex to be accessed from a remote location for the purpose of trouble-shooting or updating of the program (wherein said management computer has an interface which is connected to an external device via a network, and wherein said management computer receives an instruction from said external device via said interface).

***Allowable Subject Matter***

4. Claims 2, 3, 5, 7, 8, 10, 11, 14, and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Response to Arguments***

5. Applicant's arguments with respect to claims 1 and 6 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent 5,008,885                    Huang et al.

U.S. Patent 5,058,112                    Namitz et al.

U.S. Patent 5,428,624                    Blair et al.

U.S. Patent 6,519,718 B1                Graham et al.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

Art Unit: 2113

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C Maskulinski whose telephone number is (703) 308-6674. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MM

  
ROBERT BEAUSOLIEL  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100